LCLC Resonant Converter For Hold Up Mode Operation

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***Abstract*— In computer and telecommunication power supplies, the front end DC-DC stage is required to operate with a wide input voltage range to provide hold up time when AC voltage fails. Conventional LLC converter serving as the DC-DC stage is not suitable for this task, as the normal operation efficiency at 400Vin will be penalized once the converter is designed to achieve high peak gain, i.e. the wide input voltage range. This paper examines the operation of the LCLC converter and proposes a design methodology of LCLC converter to increase the peak gain without sacrificing the efficiency at normal input voltage condition. In normal operation, LCLC converter behaves like an LLC converter with large magnetizing inductor L_m, hence the magnetizing inductor current is reduced. During the hold-up condition, by reducing the switching frequency, the equivalent magnetizing inductive reactance of the LCLC converter will reduce more than that of the LLC converter, thus the converter enjoys higher peak gain. To verify the effectiveness of the LCLC converter for hold up operation, analysis will be presented, a design method based on capacitor voltage stress will be introduced, and experimental results from a 250V-400V input and 12V/500W prototype will be demonstrated.**

Keywords—LLC resonant converter; telecommunication; hold up; wide voltage range

I. INTRODUCTION

Hold-up problem in computer and telecommunication power systems has attracted increasing research focus in recent years. The typical structure of the front end converter is shown in Fig. 1. The Power Factor Correction (PFC) stage converts the AC line voltage into 400V DC bus which is further converted by the DC-DC stage into the 12V DC bus.

Hold-up problem (Fig. 2) describes as when the input AC power is lost, the output 400V DC bus voltage of the PFC stage will continuously drop as the energy storage capacitor discharges. The DC-DC stage converter is then required to operate with a bus voltage that is lower than the designed level (i.e. 400V), so that a period of time can be saved for the UPS to react. In this way, the load or the end converters will not 'feel' the input AC interrupt. Usually the hold-up period is within tens of milliseconds [1].

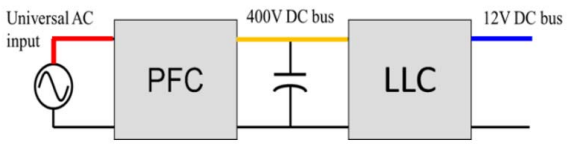

Fig. 1. Structure of the front end converter

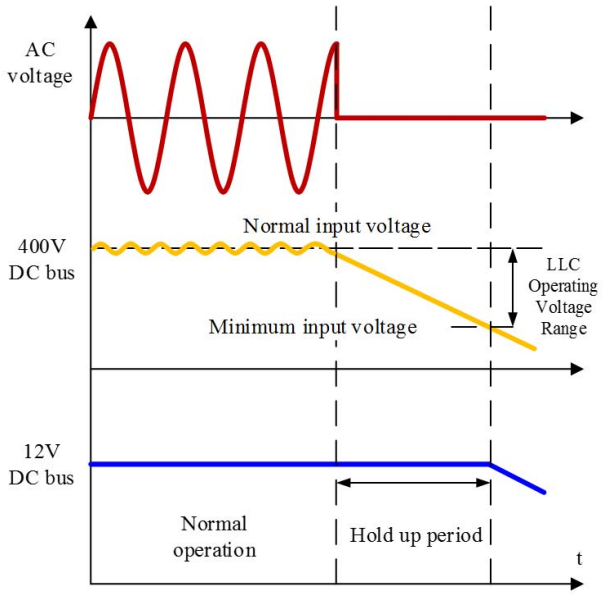

Fig. 2. Process of the Hold-up operation

LLC resonant converter is widely used as the DC-DC stage converter due to its high efficiency as a result of the inherent zero voltage switching (ZVS) for the primary MOSFETs and zero current switching (ZCS) for the secondary diodes. However, conventional LLC converter is not suitable to be designed with hold-up ability. It is widely acknowledged that if the LLC converter is designed to achieve wide input voltage range, a small magnetizing inductor value should be used. Such design will lead to severe circulation loss and conduction loss in the primary side for normal operation at 400V input.

To solve this hold-up problem, several improving methods based on LLC topology have been proposed.

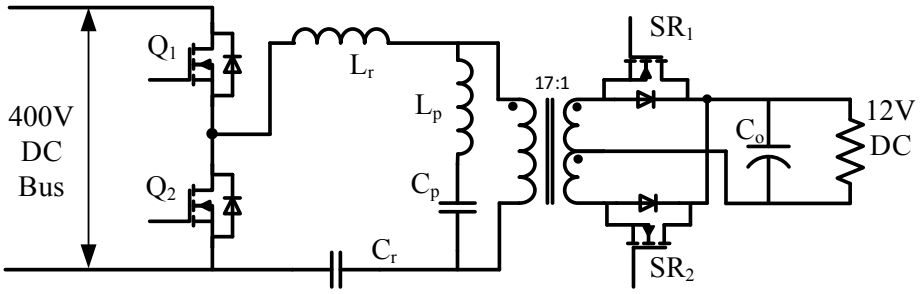

Fig. 3. LCLC converter topology with center tapped transformer and SR

Among them, the most straightforward way is to employ a cascaded structure with a baby boost converter [2]. However, the additional power diode will reduce the efficiency at normal operation. Besides, the two stage configuration is more complicated, and consequently costly.

There is a category of approaches solving the hold-up problem by utilizing auxiliary windings on the secondary side of the main transformer [3], [4]. Generally the switch-controlled auxiliary windings will be activated for power transmission when the input voltage drops, so that larger turns-ratio will increase the voltage conversion ratio to achieve hold-up state operation. The discrete design for normal state and hold-up state operation can maintain the nominal efficiency at 400V input voltage, and can limit the frequency variation within a required range. However, the critical issue of such design is the non-zero DC magnetizing current in the transformer, which increases the maximum flux density and calls for larger transformer volume. Besides, usually the main transformer is the most bulky and lossy part of the converter, thus adding a winding makes it more difficult to optimize the transformer from the efficiency improvement point of view.

By driving the Half-bridge (HB) MOSFETs with asymmetric pulse-width modulation (APWM) rather than conventional frequency modulation (FM), LLC converter can achieve increased output-to-input voltage gain without any additional components [5]. This method, however, suffers from limited peak gain enhancement as well as the DC magnetizing current in the transformer. It is published that APWM LLC converter is limited for applications below 100W.

More recently, a few methods are proposed to add switches on either primary side or secondary side to adopt Boost PWM discontinuous current mode (DCM) control scheme on a LLC topology [6]–[9]. For those methods, the positive aspect is that normal efficiency remains uninfluenced compared with a conventional LLC which is optimized for 400V input voltage. However, during the hold-up time, as the converter is operating at DCM, the conduction time is far less than 50% cycle period, such that the secondary side suffers from high RMS value of the triangle current. Furthermore, most of the topologies adopting discontinuous Boost concept cannot be applied to 12V output applications where synchronous rectifier (SR) is a must.

In this paper, the LCLC converter is revisited from increasing the voltage gain point of view to solve the hold-up problem while avoiding the aforementioned issues. The main benefits of the LCLC converter include: first, in normal operating conditions, the equivalent magnetizing inductor can be designed with a large value, so that low magnetizing current can be achieved. Second, LCLC is suitable for 12V output applications with SR. Moreover, LCLC converter avoids input voltage detection and sudden operation changes, resulting in an easy-to-control converter with high reliability. This paper is organized as follows: Section II describes the working principle of LCLC converter from DC voltage gain point of view; Section III discusses a design methodology according to capacitor voltage stresses; Section IV demonstrates the experimental results; and Section V concludes the paper.

II. Operation Principle Of LCLC Converter From DC Gain Point of View

The LCLC converter is shown in Fig. 3. As compared with LLC converter, a capacitor is connected in series with the magnetizing inductor (usually of large value). If the value of the capacitor C_p is select such that the resonant frequency of L_p and C_p is lower than the switching frequency over the entire operation range, then when switching frequency reduces, the impedance of L_p and C_p branch will still maintain as inductive and will reduce more quickly as compared with that of the LLC converter. As a result, LCLC converter achieves higher gain at when input voltage is low. At nominal input voltage, the switching frequency is higher and the impedance of the L_p and C_p branch will be high, which achieve higher efficiency. The detailed analysis will be given below.

Fig. 4 shows a typical gain curve versus switching frequency of LCLC converter. Conventional frequency modulation can still be used. It should be noted that L_p and C_p forms a resonance pair on the parallel branch except for the L_r, C_r pair on the series branch. The parallel resonant frequency should be designed lower than the series resonant frequency. The operating switching frequency should be limited within the series resonant frequency and the parallel resonant frequency, such that the impedance of the parallel branch remains inductive, and ZVS for HB FETs and ZCS for SR FETs can be achieved respectively.

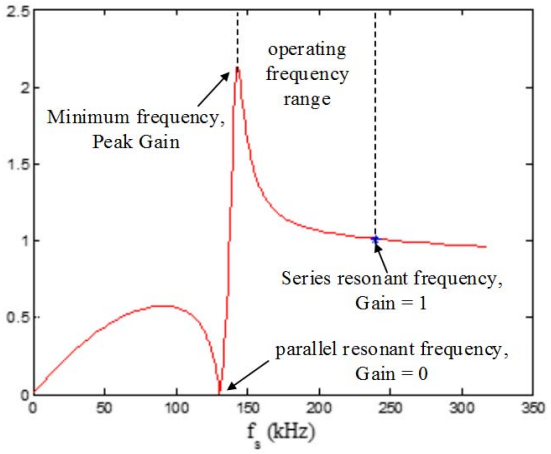

Fig. 4. Typical gain curve of LCLC converter

It is well known that the magnetizing inductance L_m determines the peak voltage gain of an LLC converter when the resonant inductor is selected. According to First Harmonics Approximation (FHA) method [10], [11], for given L_r and C_r, smaller L_m will achieve higher voltage gain. However, from the efficiency optimization point of view, larger L_m results in reduced magnetizing current and hence higher efficiency. For hold-up applications, it is desired that the converter operates with a large L_m at nominal (high) input voltage, and can automatically reduce the L_m value in case the input voltage drops. Such characteristic can be achieved by the LCLC converter.

If the values of L_p and C_p are selected so that it is inductive over entire switching frequency range, an LCLC converter can be equivalent to a set of LLC converters with same L_r, C_r while different L_ms. At a specific switching frequency, the equivalent magnetizing inductor L_{m_eq} can be calculated by (1).

$$L_{m\_eq}(f_s) = L_p - \frac{1}{(2\pi f_s)^2 C_p} \tag{1}$$

Fig. 5 illustrates the relationship between equivalent L_m and switching frequency f_s, using the parameters in Table 1 and Table 2. The DC gain of LCLC converter is determined by (2), in which L_{m_eq} is derived from (1).

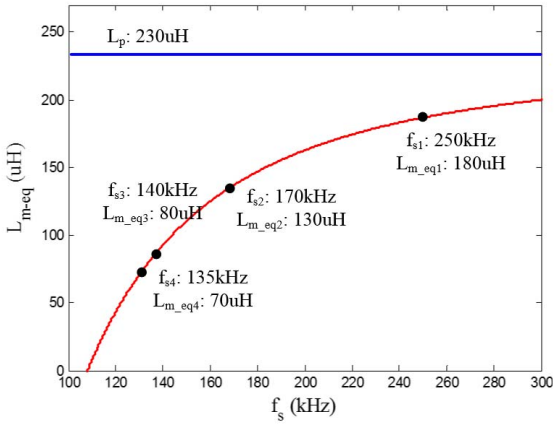

Fig. 5. Equivalent L_m changing with f_s

$$G = \frac{1}{\sqrt{\left(1+\frac{L_r}{L_{m\_eq}}-\frac{L_r}{L_{m\_eq}}\left(\frac{f_r}{f_s}\right)^2\right)^2+\left(\frac{\pi^2}{8n^2}Q\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)\right)^2}} \tag{2}$$

In Fig. 6, red curve shows the voltage gain curve of LCLC converter and blue curves show the voltage gain curves of LLC converters with several different L_m values.

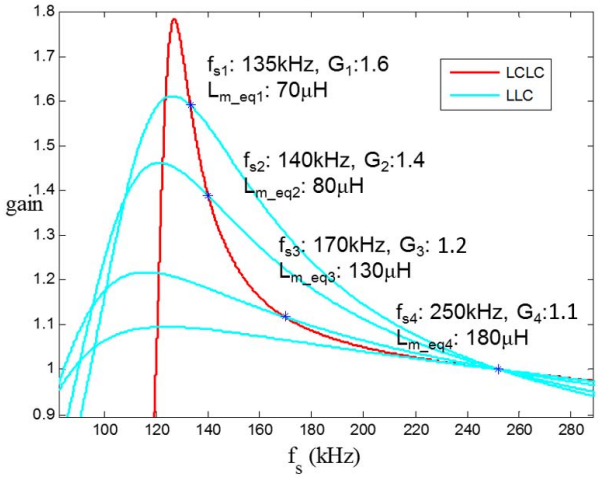

Fig. 6. LCLC and equivalent LLC gain curves

From Fig. 5 and Fig. 6, it is observed that for LCLC converters:

1. At input voltage of 400V (normal operating condition), the converter operates at the series resonant frequency 250 kHz. The corresponding gain is unity based on FHA analytical method. The equivalent L_m at the series resonant frequency is 180μH. This comparably large L_m reduces both conduction loss and switching loss in the primary side, thus the efficiency for normal operation is high.
2. When the input voltage drops, the switching frequency also reduces and the equivalent L_m is reduced. At 135 kHz, the equivalent L_m is 70μH. Peak gain of this set of parameter increases to 1.6 (from 1.1 with 180μH), which means the input voltage can go as low as 250V.

III. DESIGN METHODOLOGY

It can be observed from the FHA analysis that if the switching frequency variation is kept to a narrow range, a small resonant capacitor should be used. Correspondingly, the AC voltage stress on the capacitor can be as high as 1KV in 500W and above applications. High voltage stress on the capacitor not only increases the cost, but also reduces the reliability. Especially when C_p is added, it is essential to balance the voltage stresses on both capacitors to achieve optimal capacitor utilization. Based on that criteria, a design methodology based on the capacitor voltage stress is used in this paper.

To help illustrate the design methodology, a design example is given in the following section. The design is based on a 250V-400V input, 12V/500W output application. The turns-ratio of the transformer is selected as 17:1 to ensure that the voltage gain at 400V is unity. The series resonant frequency is chosen at 250 kHz. The detailed design steps are given as follows:

A. Assumption of minimum switching frequency

The design procedure starts with the selection of the minimum switching frequency, which determines the maximum current stress and voltage stress for capacitors. It is also assumed that peak gain of the LCLC converter is critically achieved at minimum switching frequency (i.e. consider no margin for voltage gain). According to the pre-determined series resonant frequency, a reasonable minimum switching frequency of 150 kHz is chosen.

B. Cr selection

Once the minimum switching frequency is selected, the resonant current for 250V operation can be calculated. At minimum switching frequency, theoretically the current in the HB FETs is critically in phase with the input square-wave voltage. That is to say, in half switching cycle, the resonant current will charge the resonant capacitor C_r from its minimum to its maximum voltage [12]. The charging process is shown in Fig. 7. Thus, given a capacitor value C_r, the voltage stress V_{Cr} can be calculated by (3) and (4). Considering that the maximum AC voltage ratings for capacitors are around 400V at 150 kHz in (5), the minimum value of C_r can be obtained. Generally, small Cr value is preferred in terms of reducing the circulating loss.

$$E_{\text{half\_cycle}} = \frac{V_o^2}{R_L f_{\min}} = \frac{1}{2} V_i Q_{in} \tag{3}$$

$$V_{Cr\_pp} = \frac{Q_{\text{in}}}{C_r} \tag{4}$$

$$V_{Cr\_pk} = \frac{1}{2} V_{Cr\_pp} < 400V \tag{5}$$

C. L_r selection

Considering the pre-determined resonant frequency, once the resonant capacitor is selected, the resonant inductor can be obtained in (6). Large value of L_r is preferred, because to achieve the required gain, the magnetizing inductor L_m can be chosen with a large value, which means the magnetizing current in the primary side is low during the whole input voltage range.

$$\mathrm{L}_r = \frac{1}{(2\pi f_r)^2 \cdot C_r} \tag{6}$$

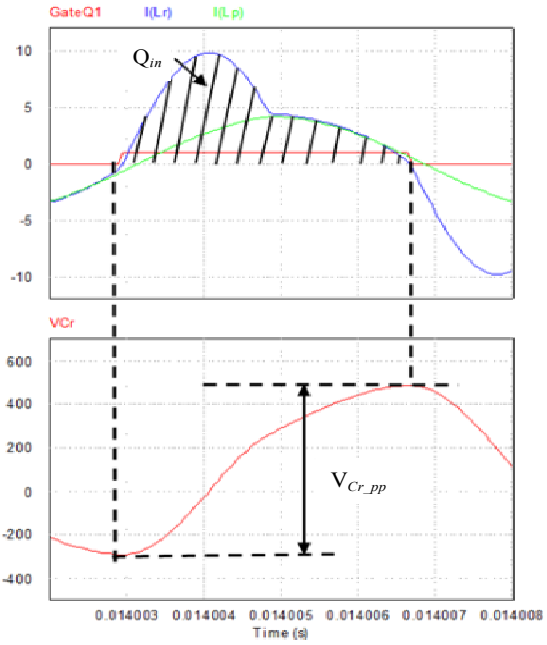

Fig. 7. C_r charging curve at minimum frequency

D. C_p selection

The critical criterion for C_p selection is the voltage V_{Cp}. If C_p is of small value, L_p can be picked with a large value, which reduces the circulating current and improves the efficiency. However, the voltage rating of the capacitor limits the minimum capacitance.

Fig. 8 shows the FHA model of the LCLC converter. V_o is the voltage across the equivalent load R_{ac}. To reach the peak gain at 1.6 for 250V input, the equivalent L_m should be 70μH according to FHA analysis. Based on this, the parallel current can be calculated in (7), so that minimum parallel capacitance can be calculated in (8), considering the maximum voltage ratings in (9).

It should be noted that, until now, the calculated peak gain frequency may not match with the assumed minimum switching frequency 150 kHz. Two to three iterations might be needed to obtain the final value for the actual peak gain frequency and C_p value. In the iteration, C_r and L_r might need slight modification to match the assumed peak gain and its frequency.

$$i_p = \frac{v_o}{X_p} = \frac{2\sqrt{2}}{\pi} \cdot \frac{nV_o}{2\pi f_{s\_pk} L_{m\_\text{eq}}} \tag{7}$$

$$v_{Cp} = i_p X_{Cp} = i_p \frac{1}{2\pi f_{s\_pk} C_p} \tag{8}$$

$$\sqrt{2} v_{Cp} < 400V \tag{9}$$

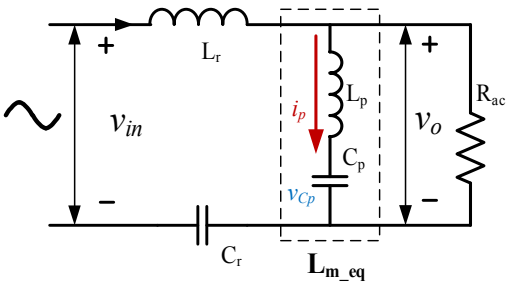

Fig. 8. FHA model of LCLC converter

E. L_p selection

For a given C_p, there is one and only one L_p that pairs with it, to critically achieve the required peak gain at minimum input voltage (250V in this case). Thus, L_p can be chosen as long as their equivalent L_m is as calculated in the last step (70μH in this case).

Considering a reasonable voltage gain margin, the final LCLC resonant tank design is as in Table 1.

TABLE I. PARAMETER DESIGN OF LCLC CONVERTER

L_r	16.5 μH	**L_p**	230 μH
C_r	23.5 nF	**C_p**	9.4 nF
f_r	250 kHz	***f_p***	110 kHz

IV. EXPERIMENTAL RESULTS

To verify the effectiveness of LCLC topology and the design method, a prototype is built to operate at 250V-400V input voltage under rated 12V/500W load. Detailed design specification is shown in Table 2. The dead time between the top switch and the bottom switch of the half bridge is set at 400ns.

TABLE II. DESIGN SPECIFICATION OF LCLC CONVERTER

V_{in}	400V-250V
V_o	12V
P_o	500W
C_o	860uF (330uF*2+100uF*2)
T_x	17:1
L_{lkg}	5uH
HB MOSFET	IPW60R190C6 (600V,20A,170mΩ)
SR	SiRA00DP (30V,100A,1mΩ)

Fig. 9 - Fig. 12 presents the steady state waveforms of the LCLC converter at 400V/250V input, 40A/20A load respectively. Due to the leakage inductance of the main transformer, the actual switching frequency is a little lower than the designed. At 400V operation, the equivalent L_m is 180uH, and the magnetizing current is hence limited, and high efficiency at nominal state can be achieved. At 250V, the magnetizing current is large, which implies the equivalent L_m is reduced to accommodate the low input voltage.

Fig. 9 shows the steady state waveforms at 400V input voltage, under 12V/40A full load condition.

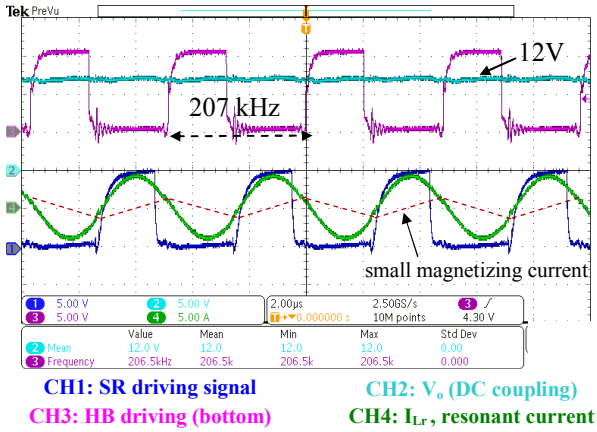

Fig. 9. 400V input, 12V/40A output steady state waveform

Fig. 10 shows the steady state waveforms at 250V input voltage, under 12V/40A full load condition.

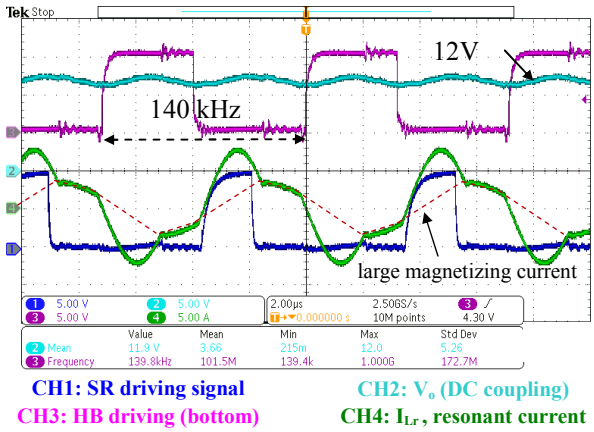

Fig. 10. 250V input, 12V/40A output steady state waveform

Fig. 11 shows the steady state waveforms at 400V input voltage, under 12V/20A half load condition.

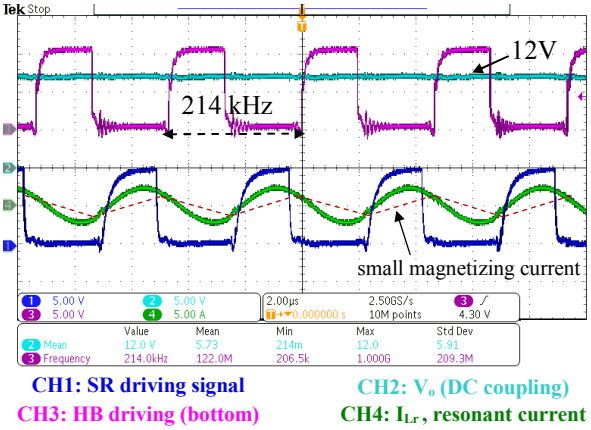

Fig. 11. 400V input, 12V/20A output steady state waveform

Fig. 12 shows the steady state waveforms at 250V input voltage, under 12V/20A half load condition.

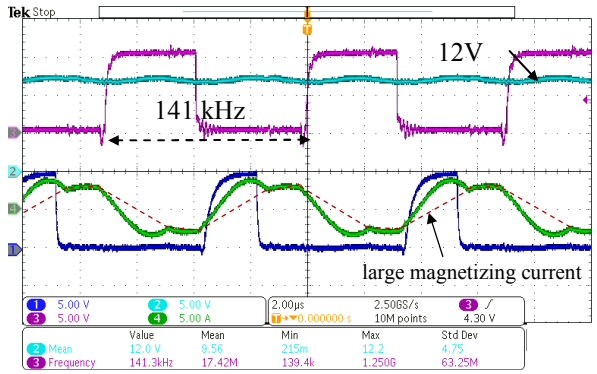

Fig. 12. 250V input, 12V/20A output steady state waveform

Fig. 13 and Fig. 14 shows the output voltage response to the input voltage drop. Under full load condition, the output voltage can be maintained at 12V even when the input voltage drops to 220V.

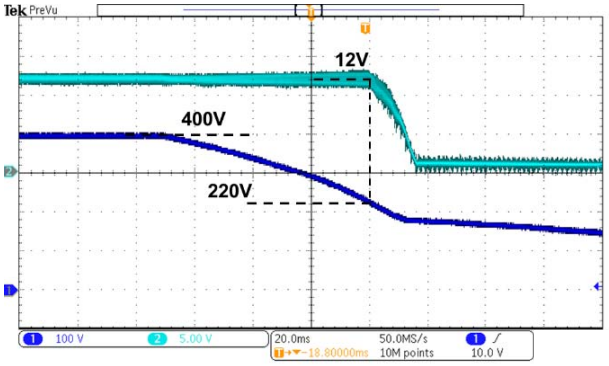

Fig. 13. Hold-up test under full load

Under half load condition, the output voltage can be maintained at 12V with as low as 200V input voltage.

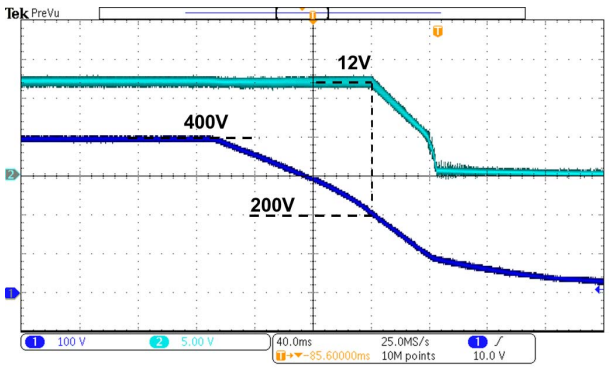

Fig. 14. Hold-up test under half load

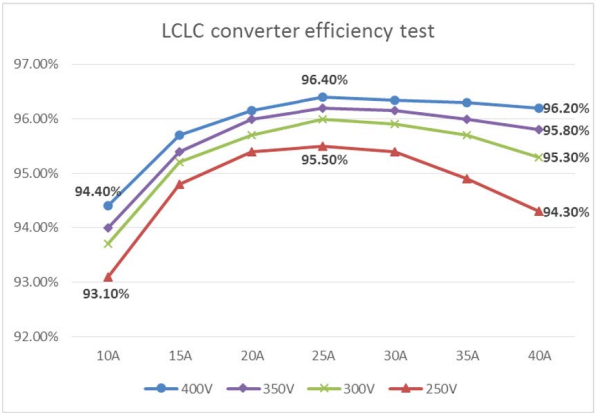

Fig. 15. efficiency curves of different input voltage level v.s. load

Fig. 15 shows the measured efficiency at different input voltages - 250V, 300V, 350V and 400V. The highest efficiency achieved is 96.4% at 400V input, 60% load, which is a reasonable outcome. For 400V input, full load condition, the achieved efficiency is 96.2%. As the input voltage reduces, the equivalent L_m is reduced, the circulation loss and conduction loss increases, the efficiency is thus reduced. For 250V condition, the highest efficiency is 95.5% at 60% load. For full load, the measured efficiency is 94.3%.

V. CONCLUSION

This paper provides a new method to solve the hold-up problem in telecommunication power applications. LCLC converter achieves high efficiency in normal operation condition, and wide operational input voltage range to satisfy the hold-up requirement. Besides, LCLC converter enjoys high reliability and simple control as no active components are added to conventional LLC converter. A design methodology focusing on the capacitor voltage stress is proposed to achieve optimal capacitor utilization. A 500W prototype is built to verify the effectiveness of the topology and the design method.

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